

CODE	COURSE NAME	CATEGORY	L	T	P	CREDIT
EET206	DIGITAL ELECTRONICS	PCC	3	1	0	4

Preamble : Nil

Prerequisite : Nil

Course Outcomes : After the completion of the course the student will be able to:

CO 1	Identify various number systems, binary codes and formulate digital functions using Boolean algebra.
CO 2	Design and implement combinational logic circuits.
CO 3	Design and implement sequential logic circuits.
CO 4	Compare the operation of various analog to digital and digital to analog conversion circuits.
CO 5	Explain the basic concepts of programmable logic devices and VHDL.

Mapping of course outcomes with program outcomes

	PO 1	PO 2	PO 3	PO 4	PO 5	PO 6	PO 7	PO 8	PO 9	PO 10	PO 11	PO 12
CO 1	3	1										
CO 2	3	3	2									
CO 3	3	3	2									
CO 4	3	2	1									
CO 5	3	2	2		2							

Course Level Assessment Questions

Course Outcome 1 (CO1):

1. Convert one number system to another form.-Binary, decimal, octal and hexadecimal
2. Arithmetic's using of a 2's complement method?
3. Binary and BCD arithmetic's.
4. Reduce the Boolean expression.
5. Develop logic circuits using Universal gates.
6. Reduce the Boolean expression using Boolean laws.
7. Describe the logic levels used in TTL logic system.

Course Outcome 2 (CO2):

1. Convert an SOP form to a POS form and vice-versa?
1. Boolean expression simplification using K map.
2. Design full adder using NAND gates alone.
3. Draw and explain the circuit of carry look ahead adder circuit.
4. Discuss how the look ahead carry adder speed up the addition process?
5. Design of i) Half adder ii) Full adder iii) Full subtractor using gates

6. Differentiate priority encoder and ordinary encoder.
7. Explain the use of the enable input in a decoder?
8. Explain odd parity generator and even parity generator.
9. Differentiate between Multiplexers and De- Multiplexers.
10. Design an 8421 to 2421 BCD code converter and draw its logic diagram.

Course Outcome 3(CO3):

1. Explain different types of flip-flops and its application areas.
2. Design various counter circuits.
3. Describe a level triggered flipflop and compare it with an edge triggered flipflop?
4. Discuss master slave flipflop?
5. Design a mod-7 asynchronous counter using J-K flipflop.
6. Distinguish ring counter from Johnson counter.
7. Explain various types of shift register?
8. Differentiate between a counter and a shift register?

Course Outcome 4 (CO4):

1. Determine the number of output voltages that can be produced by an 8 bit ADC.
2. Write the advantage of the R-2R ladder DAC over the weighted resistor type DAC?
3. Which one is the fastest ADC and explain why?
4. Compare PLA and PAL?
5. Describe programmable logic array and differentiate it from ROM?

Course Outcome 5 (CO5):

1. Differentiate between Moore and Mealy machine?
2. Explain the function of mealy machine
3. Code implementation of simple circuits using Verilog
4. Explain FPGA and state its applications?



Model Question Paper

QP Code:

Pages: 2

Reg No: _____

Name: _____

**APJ ABDUL KALAM TECHNOLOGICAL UNIVERSITY FOURTH SEMESTER
B.TECH DEGREE EXAMINATION,
MONTH & YEAR**

Course Code: EET 206

Course Name: DIGITAL ELECTRONICS

Max. Marks: 100

Duration: 3 Hours

PART A**Answer all Questions. Each question carries 3 Marks**

1. Translate the gray code 10110010101 to binary number.
2. Express the decimal number -31 as an 8 bit binary number in sign magnitude form, 1's complement form and 2's complement form.
3. Simplify the Boolean expression $AB + \overline{AC} + A\overline{B}C(AB + C)$.
4. Develop the standard Sum of Products(SOP) for the logic expression $F(A,B,C,D) = AB + \overline{A}B\overline{D} + B\overline{C}D$
5. Differentiate between Multiplexers and De- Multiplexers.
6. Realize a 2-bit comparator.
7. How does a J-K Flip Flop differ from an S-R Flip Flop in its operation?
8. What are PRESET and CLEAR inputs?
9. Draw the schematic of a successive approximation A/D converter.
10. Differentiate PLA and PAL circuits (10 x 3 = 30)

PART B**Answer any one full question from each module. Each question carries 14 Marks****Module 1**

11. (a) Why is two's - complement method of representing signed integer numbers preferred over ones complement in digital circuits? What is range of numbers that can be represented using two's complement with four bits? (10)
- (b) Represent the decimal number 3.248×10^4 in single precision IEEE binary format (4)
12. (a) Explain the working of a TTL NAND gate with the help of internal diagram. (10)
- (b) Compare CMOS and TTL performance. (4)

Module 2

13. (a) Make use of a 4 variable K map and simplify $F(A,B,C,D) = \sum_m(1,4,9,10,11,12,14) + d(0,8,13)$. Realize the function using NAND gates only. (10)
- (b) Design a half adder circuit and realize using NAND gates only. (4)
14. (a) Realize a look-ahead-carry adder. (8)
- (b) Construct the truth table for a full adder. Reduce it using K map. Implement it using logic gates. (6)

Module 3

15. (a) Explain the even parity method for error detection. (8)
- (b) Use a 4 x 1 MUX to implement the logic function $F(A,B,C) = \sum_m(1,2,4,7)$. (6)
16. (a) What is the purpose of decoder? Explain the functioning of a BCD to Decimal Decoder circuit. (8)
- (b) Explain the architecture of ALU with the help of a block diagram (6)

Module 4

17. (a) Realize an S-R flip flop using a D flipflop. (10)
- (b) What is the race around condition of a J-K flip flop? How can it be avoided? (4)
18. (a) Design a Synchronous Mod-6 Counter using J-K FFs (8)
- (b) Draw a parallel in -serial out (PISO) register and explain its working. (6)

Module 5

19. (a) Differentiate between Moore and Mealy machine? Compare them with the help of logic diagrams. (10)
- (b) What is the advantage of the R-2R ladder DAC over the weighted resistor type DAC? (4)
20. (a) Explain FPGA and state its applications? (8)
- (b) Design and implement a half adder using Verilog. (6)

Module 1

Number Systems and Codes: Binary, Octal and hexadecimal conversions- ASCII code, Excess -3 code, Gray code, BCD, Error detection codes-Parity method.

Signed numbers- representation, addition and subtraction, Fixed point and floating-point representation.

Logic gates, Universal gates, TTL and CMOS logic families-Internal diagram of TTL NAND gate and CMOS NOR gate. Comparison of CMOS and TTL performance.

Module 2

Boolean Laws and theorems, Sum of Products method, Product of Sum method – K map representation and simplification(up to four variables) - Pairs, Quads, Octets, Don't care conditions.

Combinational circuits: Adders -Full adder and half adder, Subtractors- halfsubtractor and fullsubtractor, 4 bit parallel binary adder/subtractor, Carry Look ahead adders.

Module 3

Comparators, Parity generators and checkers, Encoders, Decoders, , BCD to seven segment decoder, Code converters, Multiplexers, Demultiplexers, Architecture of Arithmetic Logic Units (Block schematic only).

Module 4

Flip-Flops, SR, JK, D and T flip-flops, JK Master Slave Flip-flop, Preset and clear inputs, Conversion of flip-flops.

Registers -SISO, SIPO, PISO, PIPO.

Up/Down Counters: Asynchronous Counters – Modulus of a counter – Mod-N counters
Ring counter, Johnson Counter

Synchronous counters, Design of Synchronous counters.

Module 5

State Machines: State transition diagram, Moore and Mealy Machines

Digital to Analog converter –Specifications, Weighted resistor type, R-2R Ladder type. Analog to Digital Converter – Specifications, Flash type, Successive approximation type.

Programmable Logic Devices - PAL, PLA, FPGA (Introduction and basic concepts only)
Introduction to Verilog, Implementation of AND, OR, half adder and full adder.

Note: Course assignments may be given in Verilog programming

Text Books

1. Floyd T.L, Digital Fundamentals, 10/e, Pearson Education, 2011.
2. C.H.Roth and L.L.Kimney Fundamentals of Logic Design, 7/e, Cengage Learning, 2013.
3. Mano M.M, Logic and Computer Design Fundamentals, 4/e, Pearson Education.
4. A Anand Kumar, Fundamental of Digital Electronics ,Prentice Hall
5. Roy Chaudari ,Linear Integrated Circuits, New Age International Publications
6. S. Salivahanan , Digital Circuits and Design, Oxford University Press

Reference Books

1. Donald P. Leach, Albert Paul Malvino and GoutamSaha, Digital Principles and Applications, 8/e, by McGraw Hill.
2. Tocci R.J. and N.S.Widmer, Digital Systems, Principles and Applications, 11/e, Pearson Education.
3. John F. Wakerly, Digital Design: Principles and Practices, 4/e, Pearson, 2005.
4. Taub& Schilling: Digital Integrated Electronics, McGraw Hill, 1997.

Course Contents and Lecture Schedule

No	Topic	No. of Lectures
1	Number systems and Binary codes ¹⁰	
1.1	Introduction, Binary, Octal and hexadecimal conversions	2
1.2	ASCII code, Excess -3 code, Gray code, BCD.	1
1.3	Error detection codes –Parity Codes.	1
1.4	Signed numbersrepresentation, addition and subtraction	1
1.5	Fixed point and floating-point representation	2
1.6	Logic gates and universal gates	1
1.7	TTL and CMOS logic families-Internal diagram of TTL NAND gate and CMOS NOR gate. Comparison of CMOS and TTL performance.	2
2	Boolean Algebra and Adders ⁹	
2.1	Boolean Laws and theorems.	1
2.2	Standard forms and canonical forms, Sum of Products method, Product of Sums method.	2
2.3	K-map representation and simplification (upto four variables) -Pairs, Quads, Octets, Don't care conditions. Realisation using universal gates.	2
2.4	Adders - Full adder and half adder – Subtractors, half subtractor and full subtractor.	2
2.5	4-bit parallel binary adder/subtractor.	1
2.6	Carry Look-ahead adders.	1

3	Combinational Logic Circuits	9
3.1	2- and 4-bit magnitude comparator.	2
3.2	Parity generators and checkers.	1
3.3	Encoder, Decoder-BCD to decimal and BCD to seven segment decoders.	2
3.4	Realisation of Code converters.	1
3.5	Multiplexers and implementation of functions, Demultiplexers	2
3.6	Architecture of Arithmetic Logic Units (Block schematic only)	1
4	Sequential circuits10	
4.1	Flip-Flops, SR, JK, D and T flip-flops, JK Master Slave Flip-flop, Preset and clear inputs	2
4.2	Conversion of flip-flops.	2
4.3	Registers -SISO, SIPO, PISO, PIPO.	1
4.4	Up/Down Counters: Asynchronous Counters – Modulus of a counter – Mod-N counters.	2
4.5	Ring counter, Johnson Counter.	1
4.6	Design of Synchronous counters	2
5	State Machines, D/A and A/D converters and PLDs7	
5.1	State Machines: State transition diagram, Moore and Mealy Machines	1
5.2	Digital to Analog converter – R-2R ladder, weighted resistors.	1
5.3	Analog to Digital Converter - Flash ADC, Successive approximation.	1
5.4	Programmable Logic Devices - PAL, PLA-function implementation - FPGA (Introduction and basic concepts only).	2
5.5	Introduction to VHDL, Implementation of AND, OR, half adder and full adder.	2